Analyzing Throughput of Power and Thermal-constraint Multicore Processor under NBTI Effect

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ABSTRACT
NBTI (Negative Bias Temperature Instability) which can degrade the switching speed of PMOS transistors has become a major reliability challenge. In this paper, we investigate the throughput impact of NBTI on power and thermal-constraint multicore processors and show up to 30% degradation when both process variation and NBTI are considered. Then we evaluate the effectiveness of core rotation, adaptive voltage scaling and adaptive body biasing to improve the throughput of power and thermal constrained multicore processors. Our experimental results demonstrate 11.1% improvement in \( V_{DD} \) is sufficient to guarantee throughput after 10-yr NBTI influence when process variation is not considered. In contract, ABB technique is not able to recover throughput loss caused by NBTI.

Categories and Subject Descriptors:
C.4 [Performance of Systems]: Design studies

General Terms
Performance, Reliability

Keywords
NBTI, Process Variation, Multicore Processor

1. INTRODUCTION
The power wall has changed the development of microprocessors from a single-core design to many smaller cores. Multicore processors can provide higher throughput when running highly parallelized applications. However, not many existing applications offer high parallelism and not all of the cores are active at the same time. In the case of power- and thermal-constrained multicore processors, these idle cores can be turned off to reduce power dissipation and to provide power and thermal headroom for the active cores. Thus, the frequency of active cores can be increased to provide higher system throughput by using dynamic voltage and frequency and adaptive body biasing [1, 2].

Meanwhile, as technology advances, reliability is becoming a more serious issue. Two of the major reliability culprits are process variation (PV) and Negative Bias Temperature Instability (NBTI). PV is mainly caused by variation in process parameters and variations in the dimensions of the devices due to the limited resolution of photolithography. It can be categorized into die-to-die (D2D) and within-die (WID) variations. D2D variations affect all transistors in a die equally, while WID variations induce different electric characteristics across a die. Both can cause substantial variations on transistor delay and leakage within and across a die. Furthermore, individual cores are becoming small enough that spatially correlated WID process variations will cause core-to-core (C2C) frequency and leakage power variations[3].

NBTI occurs due to the disassociation of the Si-H bond and continuous generation of interface traps when PMOS transistors are under stress (\( V_{GS}=V_{DD} \)). The increased threshold voltage of the PMOS transistor decreases the drive current. Hence, the circuit speed degrades and the critical paths may no longer be able to sustain the required time. Much of the existing NBTI-related work has focused on gate and micro-architectural levels [4-6] and has shown insignificant performance degradation due to NBTI; however, few studies have been done on the multicore processors. In addition, the process variation causes non-uniform performance degradation on each core, and thus throughput analyses of multicore processor become unintuitive.

In this work, we first investigate the impact of NBTI on the frequency of multicore processors with and without process variation. We analyze the throughput improvement of multicore processors using core rotation, adaptive voltage scaling, adaptive body biasing on power and thermal constrained processors under the influence of NBTI.

This paper is organized as follows: The background for NBTI models, throughput and power models for multicore processor modeling is presented in Section 2. Section 3 discusses NBTI-aware throughput analysis for multicore processor and throughput improvement. Section 4 details the experimental setup and Section 5 concludes this paper.

2. MODELS

2.1 Multicore Processor Models
This section introduces the throughput and power modeling that we adapted mainly from [1] and the NBTI models for this work.

2.1.1 Throughput Model
The well-known Amdahl’s law has been extended to model the speedup improvement of multicore processors [1, 7]. In a multicore processor, PV has caused core-to-core maximum operating frequency variation (\( F_{max} \)) and maximum frequency will be limited to the slowest core if a global clock is used. Therefore, dynamic voltage and frequency scaling (DVFS), per-core power gating (PCPG) and adaptive body biasing (ABB) techniques are proposed to improve multicore processors under power and...
thermal constraints [1, 2]. The throughput model is rewritten as follows:

\[
\text{Speedup}_{\text{enhanced}} = \frac{1}{f(V_{DD}, V_{BB}) \cdot \text{perf}(R)} + \frac{F}{f(V_{DD}, V_{BB}) \cdot \text{perf}(R) \cdot n}
\]

(1)

F is a program’s execution time that was infinitely parallelizable without overhead. \(f(V_{DD}, V_{BB})\) is the frequency of \(n\) chosen cores under supply voltage \(V_{DD}\), and body biasing voltage \(V_{BB}\). \(\text{perf}(R)\) is the performance improvement of a core when \(R\) base core equivalent (BCE) is combined to become a single core. Normally, \(\text{perf}(R)\) is close to \(\sqrt{R}\). Note that instead of \(N / R\), \(n\) is used to indicate the numbers of active cores since not all the cores need to be active at the same time.

2.1.2 Power Model
When parallelism of the workload is not high and some cores are idling, some cores can be shut down to provide extra power and thermal headroom. The active cores can instead improve performance by using AVS and ABB techniques. In this work, we adapt the power model from [1] and repeat as follows:

\[
P_{\text{tot}} = \frac{c(F,K,n)}{N/R} \cdot f(V_{DD,j}, V_{BB,k}) \cdot \left(\frac{V_{DD,j}}{f(V_{DD,TDP})}\right)^2 \sum_{j=1}^{n} l_j(V_{DD,j}, V_{BB,k}) \cdot \left(\frac{V_{DD,j}}{f(V_{DD,TDP})}\right)
\]

(2)

In this equation, \(P_{\text{tot}}\) is the power consumption and \(P_{\text{dyn, TDP}}\) is the dynamic power under TDP. Detailed definitions for \(c(F,K,n), LR\) and \(l_j(V_{DD,j}, V_{BB,k})\) can be found in [1].

2.2 NBTI Model
It has become apparent that NBTI presents a major reliability challenge. NBTI occurs when PMOS is under stress (\(V_{GS}=-V_{DD}\)). The interaction between inversion layer holes and hydrogen-passivated Si atoms breaks Si-H bond, generating interface traps. The interface traps increase the voltage threshold of PMOS transistors, causing the drive current to decrease. Hence, the circuit speed degrades and the critical paths may no longer be able to sustain the required time.

The physical mechanism of NBTI is well explained through the reaction-diffusion model with stress and recovers phases. The \(\Delta V_{th}\) predictive model is shown in Table 1. Default values for these parameters can be found in [8] and the PTM website [9]. \(A\) and \(K_s\) are functions of the vertical electrical field and the carrier concentration \((C=\exp(-E_a/kT)T_0)\). \(\delta, \xi_1\) and \(\xi_2\) are constant.

| Static | \(A\left((1 + \delta)C(t - t_o) + \sqrt{C(t - t_o)}\right)^{2n}\) |
| Dynamic Stress | \((K_s(t - t_o)^{0.5} + 2n\sqrt{\Delta V_{th}})^{2n}\) |
| Recover \(y\) | \(\Delta V_{th}\left(1 - \frac{2\xi_1 t_o + \sqrt{\xi_2 C(t - t_o)}}{2t_o + \sqrt{C}}\right)\) |

A first order approximation for the propagation delay of the gate \(T_d\) can be computed by

\[
T_d = a_0 + a_1 \Delta V_{th} + a_2 C_1
\]

(3)

The number \(a_0\) is the intrinsic delay of the gate without NBTI, and \(a_1\) and \(a_2\) are also constants. The constants in the above equation are obtained through HSPICE circuit simulation. These NBTI predictive models have been widely used to analyze the influence of NBTI on the circuit at the gate and at the architectural level. However, the impact of NBTI on the throughput of multicore processors remains unanswered.

We measure the frequency degradation on a core due to NBTI on a 24-stage FO4 inverter chain. Figure 1 shows the frequency degradation of a 24-stage FO4 inverter chain for 32nm PTM. The input signal probability is set to 0.5. We can observe more than 10% degradation on the inverter chain after the first year, and degradation is close to 17% after 10 years, which results in significant performance degradation.

\[\text{Figure 1. Frequency Degradation of an FO4 inverter chain due to NBTI}\]

3. NBTI-AWARE THROUGHPUT ANALYSIS OF MULTICORE PROCESSOR
In this section, we analyze the throughput degradation caused by NBTI effect.

3.1 Throughput Degradation Due to NBTI
Figure 2 shows the throughput degradation due to NBTI effect for a range of parallelism from F=0.2 to 0.8 without PV. Throughput degradation is 16% for F=0.8 in a 16-core processor and the average degradation is around 11%. It is obvious that NBTI can cause substantial throughput degradation, and most significant degradation occurs in the first year (12% to be specific).

Figure 3 shows the throughput degradation with both PV and NBTI. The throughput is normalized to initial throughput of multicore processor without process variation. The throughput degradation is exacerbated by NBTI. For example, when \(F=0.8\), throughput is around 82% of throughput when process variation is not modeled. With the effect of NBTI, throughput degrades to 73% after the first year and become 69% after ten years.

3.2 Throughput Improvement
In this section, three simple methods are proposed to mitigate the throughput degradation: core rotation, adaptive voltage scaling (AVS) and adaptive body biasing (ABB). It is quite often that AVS and ABB techniques are used together; hence, their improvement is discussed in the same section.

3.2.1 Using Core Rotation
One of the easiest ways to mitigate degradation is core rotation. The idea is to average the use of each core. Figure 4 compares the degradation with and without core rotation when PV is considered. A simple core rotation technique is used: each time the four fastest cores are selected to execute applications. After each year, we calculate the NBTI degradation on the chosen four cores, and
again choose four fastest cores (the four fastest cores may change due to degradation.). The result shows core rotation can achieve 4–7% throughput improvement. A more elaborate core rotation can be used to improve the effectiveness of this technique.

For example, the slowest core in Figure 5 (V_{DD} is 0.7 and V_{BB} is -0.3) is reduced to 70% of original frequency and the fastest core in Figure 5 (V_{DD} is 1.05 and V_{BB} is 0.4) is reduced to 90.7% of original frequency. This observation is important and will affect how to improve the throughput using AVS and ABB. By using the frequency information in Figure 5 and Figure 6, we can evaluate the throughput of multicore processors using Equation (1).

**3.2.2 Using AVS and ABB**

The core rotation method can only reduce degradation and multicore processors still suffer performance loss. AVS and ABB, however, can boost processor’s throughput to overcome throughput loss.

Figure 5 shows the frequency of cores, f(V_{DD},V_{BB}) with various V_{DD} (0.7 – 1.05) and V_{BB} (0.3 – 0.45) without NBTI effect, while 10-year NBTI effect is modeled in Figure 6. The frequency is normalized to the slowest core without NBTI effect. Note that process variation is not considered and all cores’ frequencies are the same. It can be seen that NBTI effect has caused more significant frequency degradation when V_{BB} and V_{DD} is lower.

Figure 7 shows the normalized power. The normalized \( P_{tot} \) increases super-linearly which is reasonable due to the CMOS power equation \( P=CV^2f \). A similar figure is done for power without NBTI effect, but now shown over here.

In order to improve throughput via AVS and ABB, we need to decide how many AVS and ABB domains need to be used. Lee et al. [1] has shown more than one ABB domains has only marginal improvement. Therefore, we only use one ABB domain in our analysis.

Figure 8 shows throughput degradation of various VDD for 10-year execution time, while Figure 9 shows throughput degradation
off various VBB for 10-year execution time. A 11.1% increase in voltage is sufficient to guarantee throughput remain higher than original and 5.5% increase can render throughput higher than original for 3-4 years. However, no ABB configuration can provide sufficient throughput for 10-yr execution. One reason is we only change body voltage of PMOS. Therefore, AVS is more effective in providing throughput improvement.

Figure 8. Throughput degradation versus execution time for a range of VDD (F=0.5, n=4)

Figure 9. Throughput degradation versus execution time for a range of VBB (F=0.5, n=4)

Figure 10. Combined throughput analysis of both VDD and VBB for 10-year execution time.

Figure 10 shows normalized throughput after 10-yr NBTI by combining AVS and ABB techniques. A dot line shows throughput is higher than initial throughput after 10 years. When VBB is 0.4, VDD only requires 0.9V to achieve 10-yr throughput improvement. A 11.1% increase in VDD is sufficient to guarantee throughput after 10-yr NBTI influence when PV is not considered. In contrast, ABB technique is not able to recover throughput loss caused by NBTI.

4. EXPERIMENTAL SETUP

Our experimental setup is similar to [1] and the key setup is mention below. Systematic variation for 100 35mm² dies is modeled using a multivariate normal distribution with a spherical spatial correlation structure. Threshold voltage and the effective length are distributed normally with zero mean and standard deviation $\sigma_{th}$ equal to 6.4% and $L_{eff}$ is 3.2%. We generate the variation map and each variation map is divided into 80x80 grid points. We use a 24 stage FO4 inverter chain to determine the maximum frequency of each grid point with $V_{th}$ and $L_{eff}$ from the variation map. The simulation is done on 32nm high performance predictive technology model (PTM) [9] and HSPICE is used to measure the maximum frequency. Each core has 64 grids and the core’s frequency is determined by the slowest grid. The threshold voltage increase caused by NBTI is done through typical NBTI models in Section 2.2. To estimate the delay of an FO4 inverter chain with AVS and ABB, the inverter chain is measured with threshold variation with various $V_{th}$ ($0.6 - 1.05$) and $V_{bb}$ ($-0.4 \sim +0.4$) domain. Hotspot is used with 0.3K/W for the convection resistance. The difference between our basic result without NBTI and [1] should be due to different transistor sizing.

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6. CONCLUSION

NBTI has become a major reliability challenge in 45nm technology and below. This paper investigates throughput impact of NBTI on power and thermal-constraint multicore processors and show up to 30% degradation when both PV and NBIT are considered. We evaluate the effectiveness of core rotation, adaptive voltage scaling and adaptive body biasing on improving the throughput of power and thermal constrained multicore processors. Experimental results demonstrate 11.1% improvement in VDD is sufficient to guarantee throughput after 10-yr NBTI influence when PV is not considered. In contract, ABB technique is not able to recover throughput loss caused by NBTI.

7. REFERENCES


[9] "Predictive Technology Model (PTM) and NBTI Model," Available at http://www.eas.asu.edu/~ptm